WHAT IS CLAIMED IS:

1. A method of erasing data of a nonvolatile semiconductor memory unit including a memory cell array which is provided with a plurality of nonvolatile memory transistors arranged in rows and columns, a plurality of word lines for selecting the rows of the memory transistors, respectively and a plurality of bit lines corresponding to the columns of the memory transistors, respectively and is divided into a plurality of memory blocks each having a set of the memory transistors, a potential generating portion for generating a potential applied to the word lines, the bit lines and substrates and sources of the memory transistors and a write/erase control portion for controlling the potential generating portion so as to erase the data in the memory transistors collectively or in units of the memory blocks, comprising the steps of:

collectively applying a preliminary write pulse to the memory transistors;

repeating, if the memory transistors are not in a first erased state, an operation of collective application of a first erase pulse to the memory transistors with change of intensity of the first erase pulse in second and subsequent application operations of the first erase pulse until the memory transistors assume the first erased state;

repeating, if the memory transistors are not in a recovered state, an operation of collective application of a write pulse to the memory transistors with change of intensity of the write pulse in second and subsequent application operations of the write pulse until the memory transistors assume the recovered state;

repeating, if the memory transistors are not in a second erased state,

an operation of collective application of a second erase pulse to the memory transistors with change of intensity of the second erase pulse in second and subsequent application operations of the second erase pulse until the memory transistors assume the second erased state; and

repeating, if the memory transistors are in an overerased state, a selective recovery operation on the memory transistors until the memory transistors are not in the overerased state.

2. The method according to Claim 1, further comprising the step of confirming application of the second erase pulse, which is added between the step of repeating the operation of collective application of the second erase pulse and the step of repeating the selective recovery operation.

3. The method according to Claim 2, wherein 0 V is applied to nonselected ones of the word lines in an erase verify operation in the step of repeating the operation of collective application of the second erase pulse and the step of repeating the selective recovery operation is executed in two stages having first-stage steps and second-stage steps.

4. The method according to Claim 3, wherein a further erase verify step is added after the second-stage steps in place of a first over-recovery verify operation in the first-stage steps and a second over-recovery verify operation in the second-stage steps.